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EXAMINER

CHEN, XIAOLIANG

ART UNIT

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/582,657	PEKKARINEN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Xiaoliang Chen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 20 January 2010.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1,4-7,10-14 and 17-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,4-7,10-14 and 17-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)         | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)         | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Amendment***

1. Acknowledgement is made of Amendment filed 01-20-10.
2. Claims 1, 4, 7, 10, 14, 21 and 22 are amended.
3. Claims 2, 3, 8, 9, 15 and 16 are canceled.

### ***Response to Arguments***

4. Since Claims 4, 10 and 14 are amended, the rejections of Claims 4, 10 and 14 under 35 U.S.C. 112 in last office action have been withdrawn.
5. Applicant's arguments with respect to newly amended parts of claims 1, 7, 21 and 22 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Objection***

6. Claims 1, 7, 10, 21 and 22 are objected because  
  
Claim 1 has the limitations "electroconductive material" in line 3, and "an electroconductive material" in line 5.  
  
Claim 7 has the limitations "electroconductive material" in line 4, and "an electroconductive material" in line 9.  
  
Claim 21 has the limitations "electroconductive material" in line 6, and "an electroconductive material" in line 7.  
  
Claim 22 has the limitations "electroconductive material" in line 4, and "an electroconductive material" in line 5.

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It is not clear whether the second of “an electroconductive material” is the same as or different from the first of “electroconductive material”.

For examining purpose only, read the first of “electroconductive material” as “an electroconductive material”, and read the second of “an electroconductive material” as “the electroconductive material”;

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1, 4-7, 10-13 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamada et al. (US6331063) in view of Nakajima (US20040067015).

**Re Claim 1**, Kamada et al. show and disclose

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An apparatus comprising:

a photoconductor (11, fig. 31) having a surface (top),

the photoconductor provided with an aperture (hole in 11 for placing LED 1, fig. 31),

a ground plane (19a, fig. 31),

Kamada et al. does not disclose

the aperture extends through said photoconductor and also provided with an electroconductive material at least around the edges of the aperture, and the electroconductive material induced on said surface of the photoconductor which material is connectable to the ground plane;

Nakajima teaches a device wherein

the aperture (216, fig. 64) extends through said photoconductor (212) and also provided with an electroconductive material (metal layer 222, fig. 64) at least around the edges of the aperture, and the electroconductive material induced on said surface of the photoconductor (fig. 64), which material (metal layer 222, fig. 64) is connectable to the ground plane;

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the through hole and the metal layer in the photoconductor as taught by Nakajima in the electronic device of Kamada et al., in order to view the light of LED brighter from front of the electronic device, and connect the metal layer to the ground plane to achieve the better shielding of the circuit chip with respect to noise ([col. 18, line 3], Kamada

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et al.), furthermore, using a blind hole or a through hole for a LED is just a designer's choice for variety design needs of the electronic device.

(Notes: "in order to conduct electrostatic discharges through the electroconductive material to the ground plane" is intended use; and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 UAPQ2d 1647 (1987).)

**Re Claim 4**, Kamada et al. and Nakajima disclose

The apparatus according to claim 1, wherein the electroconductive material (metal layer 222, fig. 64, Nakajima) induced on said surface of the photoconductor is integrated with the photoconductor (212, fig. 64, Nakajima) as the layer of electroconductive material for conducting light in the photoconductor (a transparent substrate 212 [0204], Nakajima) and for shielding the light source against electrostatic pulses (after connecting the electroconductive material to the grounding plane, see claim 1, shielding of the circuit chip with respect to noise also can be achieved [col. 18, line 3]).

**Re Claim 5**, Kamada et al. and Nakajima disclose

The apparatus according claim 1, wherein the electroconductive material is metal (metal layer 222, fig. 64) and is connectable to the ground plane through the electroconductive material (see claim 1).

**Re Claim 6**, Kamada et al. and Nakajima disclose

The apparatus according to claim 1, wherein the electroconductive material is realized on the surface of the photoconductor by means of an electroconductive film (metal film [0198], Nakajima), or by inducing chemically or electrochemically.

**Re Claim 7**, Kamada et al. show and disclose

An apparatus for shielding a component against electrostatic discharge, said apparatus comprising

a light emitting diode (1, fig. 31) and a photoconductor layer (11) for conducting light emitted by the light emitting diode,

wherein the photoconductor layer is provided with an aperture (hole in 11 for placing LED 1, fig. 31), the light emitting diode at least partly placed in the aperture inside the photoconductor layer (fig. 31),

a ground plane (19a, fig. 31),

Kamada et al. does not disclose

the aperture extends through said photoconductor layer, the photoconductor layer includes an electroconductive material, the electroconductive material at least around the edges of the aperture, and the electroconductive material is connectable to the ground plane,

Nakajima teaches a device wherein

the aperture (216, fig. 64) extends through said photoconductor layer (212, fig. 64), the photoconductor layer includes an electroconductive material (metal layer 222, fig. 64), the electroconductive material at least around the

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edges of the aperture (fig. 64), and the electroconductive material (metal layer 222, fig. 64) is connectable to the ground plane,

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the through hole and the metal layer in the photoconductor as taught by Nakajima in the electronic device of Kamada et al., in order to view the light of LED brighter from front of the electronic device, and connect the metal layer to the ground plane to achieve the better shielding of the circuit chip with respect to noise ([col. 18, line 3], Kamada et al.), furthermore, using a blind hole or a through hole for a LED is just a designer's choice for variety design needs of the electronic device.

(Notes: "in order to conduct electrostatic discharges from the photoconductor layer to the ground plane" is intended use; and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 UAPQ2d 1647 (1987).)

**Re Claim 10**, Kamada et al. and Nakajima disclose

The apparatus according to claim 7, wherein the photoconductor layer has a surface (top) and wherein the electroconductor material of the photoconductor layer is integrated as a layer of electroconductive material (metal layer 222, fig. 64, Nakajima, see claim 7) for shielding components against electrostatic pulses (after connecting the electroconductive material to the grounding plane, see

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claim 7, shielding of the circuit chip with respect to noise also can be achieved [col. 18, line 3]) and for conducting the light emitted by the light emitting diode (1, fig. 31) in the photoconductor layer.

**Re Claim 11**, Kamada et al. and Nakajima disclose

The apparatus according claim 7, wherein the light emitting diode is placed on a printed circuit board (19, fig. 31), the photoconductor layer is placed on the component side of the circuit board (fig. 31), and the electroconductive material is placed on that side of the photoconductor layer (fig. 64, Nakajima, see claim 7) that faces away from the circuit board and the electroconductive material is connectable (see claim 7) to the ground plane (19a, fig. 31) of the circuit board.

**Re Claim 12**, Kamada et al. and Nakajima disclose

The apparatus according to claim 7, wherein the electroconductive material is metal (metal layer 222, see claim 7), and it is connected to the ground plane by electroconductive material (connect to a plating ground layer [col. 3, line 61, Nakajima], see claim 7).

**Re Claim 13**, Kamada et al. and Nakajima disclose

The apparatus according to claim 7, wherein the electroconductive material is realized on the surface of the photoconductor layer by an electroconductive film (metal film [0198], Nakajima), or by inducing chemically or electrochemically.

**Re Claim 21**, Kamada et al. show and disclose

A method comprising:

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placing a light emitting diode (1, fig. 31) on a printed circuit board (19, fig. 31),

arranging a photoconductor layer (11, fig. 31) on a component side (top) of the circuit board, the photo conductor layer provided with an aperture (hole in 11 for placing LED 1, fig. 31),

a ground plane (19a, fig. 31) of the circuit board,

Kamada et al. does not disclose

the aperture extends through said photoconductor, providing an electroconductive material at least around the edges of the aperture, inducing the electroconductive material to the photoconductor layer,

Nakajima teaches a device wherein

the aperture (216, fig. 64) extends through said photoconductor, providing an electroconductive material (metal layer 222, fig. 64) at least around the edges of the aperture, inducing the electroconductive material to the photoconductor layer (fig. 64),

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the through hole and the metal layer in the photoconductor as taught by Nakajima in the electronic device of Kamada et al., in order to view the light of LED brighter from front of the electronic device, and connect the metal layer to the ground plane to achieve the better shielding of the circuit chip with respect to noise ([col. 18, line 3], Kamada

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et al.), furthermore, using a blind hole or a through hole for a LED is just a designer's choice for variety design needs of the electronic device.

(Notes: "in order to conduct electrostatic discharges from the photoconductor layer to the ground plane of the circuit board" is intended use; and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 UAPQ2d 1647 (1987).)

**Re Claim 17**, Kamada et al. show and disclose

The method according to claim 21, the circuit board (19, fig. 31) on bottom of the photoconductor layer,  
Kamada et al. does not disclose

wherein on the outermost surface of the photoconductor layer, facing away from the circuit board, there is integrated a layer of electroconductive material, which layer covers the whole surface of the photoconductor layer.

Nakajima teaches a method wherein

on the outermost surface (top) of the photoconductor layer, facing away from the circuit board, there is integrated a layer of electroconductive material (metal layer of 240, fig. 73), which layer covers the whole surface of the photoconductor layer (fig. 73).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the plating metal layer over the

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electroconductive material as taught by Nakajima in the electronic device of Kamada et al., in order to use the process method to process the plating electrode plate on the electroconductive material of the electronic device (Nakajima, Para. [0213]).

**Re Claim 18**, Kamada et al. and Nakajima disclose

The method according to claim 17, wherein the electroconductive material is induced for shielding components of the circuit board against electrostatic pulses (after connecting the electroconductive material to the grounding plane, see claim 21, shielding of the circuit chip with respect to noise also can be achieved [col. 18, line 3]) and for conducting the light emitted by the light emitting diode (1, fig. 31) of the circuit board in the photoconductor layer (11, fig. 31).

**Re Claim 19**, Kamada et al. and Nakajima disclose

The method according to claim 21, wherein the electroconductive material is metallized (metal layer 222, fig. 64, Nakajima) to the photoconductor layer and connected to the ground plane of the circuit board by electroconductive material (the electroconductive material connected to the ground plane, see claim 21).

**Re Claim 20**, Kamada et al. and Nakajima disclose

The method according to claim 21, wherein the electroconductive material is realized in the photoconductor layer by means of an electroconductive film (metal film [0198], Nakajima), or by inducing chemically or electrochemically.

**Re Claim 22**, Kamada et al. show and disclose

An apparatus comprising:

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means for providing a photoconductor (11, fig. 31) having a surface (top),  
the photoconductor provided with an aperture (hole in 11 for placing LED  
1, fig. 31),  
a ground plane (19a, fig. 31),

Kamada et al. does not disclose

the aperture extends through said photoconductor, provided with an  
electroconductive material at least around the edges of the aperture, means for  
providing the electroconductive material induced on said surface of the means for  
providing a photoconductor, which material is connectable to the ground plane,  
Nakajima teaches a device wherein

the aperture (216, fig. 64) extends through said photoconductor (212, fig.  
64), provided with an electroconductive material (metal layer 222, fig. 64) at least  
around the edges of the aperture, means for providing the electroconductive  
material induced on said surface of the means for providing a photoconductor  
(fig. 64), which material (metal layer 222, fig. 64) is connectable to the ground  
plane,

Therefore, it would have been obvious to one having ordinary skill in the  
art at the time the invention was made to use the through hole and the metal  
layer in the photoconductor as taught by Nakajima in the electronic device of  
Kamada et al., in order to view the light of LED brighter from front of the  
electronic device, and connect the metal layer to the ground plane to achieve the  
better shielding of the circuit chip with respect to noise ([col. 18, line 3], Kamada

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et al.), furthermore, using a blind hole or a through hole for a LED is just a designer's choice for variety design needs of the electronic device.

(Notes: "in order to conduct electrostatic discharges through the means for proving the electroconductive material to the ground plane" is intended use; and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

Ex parte Masham, 2 UAPQ2d 1647 (1987).)

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamada et al. in view of Nakajima , as applied to claim 7 above, further in view of Yu et al. (US7053799).

**Re Claim 14**, Kamada et al. and Nakajima disclose

The apparatus according to claim 7, further comprising the light emitting diode (1, fig. 31) is on a circuit board (19, fig. 31) and configured to illuminate, wherein the photoconductor layer (11, fig. 31) configured to conduct the light emitted by the for conducting the light emitted by the light emitting diode (1, fig. 31),

Kamada et al. and Nakajima do not disclose

the light emitting diode configured to illuminating a keypad and the photoconductor layer configured to conduct the light emitted by the light emitted by the light emitting diode to a key of the keypad.

Yu et al. teaches a device wherein

the light emitting diode configured to illuminating a keypad (an illuminated keypad [col. 3, line 31]) and the photoconductor layer configured to conduct the light emitted by the light emitted by the light emitting diode to a key (an illuminated keypad and button [col. 3, line 31]) of the keypad.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the LED and the photoconductor layer of Kamada et al. to illuminate the transparent keypad as taught by Yu et al., in order to provide effective light illumination the transparent keypad in a dark environment (Yu et al. col. 6, line 22-52).

### ***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US-20010049207 US-20020113934 US-3843851 US-3869637 US-3881921 US-5060595 US-5105238 US-5349346 US-05461377 US-7553088.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiaoliang Chen whose telephone number is (571)272-9079. The examiner can normally be reached on 8:00-5:00 (EST), Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jinhee Lee can be reached on 571-272-1977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Xiaoliang Chen  
Examiner  
Art Unit 2841

/Tuan T Dinh/

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Primary Examiner, Art Unit 2841